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WHITE PAPER

Debugging Point-to-Point Resistance Using Contribution by Layer in IC Validator PERC

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Introduction

PERC Point-to-point resistance (P2P resistance) functionality is a crucial EDA technology to enable complex P2P effective resistance measurement along ESD paths in automation for foundry qualified ESD/Latch-up checker or in-house custom checker. This technology is applied to the entire chip, block, and IP designs on cell or transistor level layout database. Since the ESD path count could grow to thousands or even ten thousand, it is vital that the ESD path-oriented R extraction and distributed matrix solving capability has outstanding performance. This technology does not estimate P2P resistance using shortest or longest path schemes, but instead uses an accurate simulation focused on the critical layout polygons of ESD paths, including the P/G network. The P2P resistance measurement yields result in effective resistance (ohms) for each path measured. That result is a lumped resistance value reflecting all interconnect polygon layers between Source (current injection) and Sink (current Sink). Although the P2P resistance value gives users immediate information on how effective the ESD path behaves in discharging an ESD surge, a violated P2P resistance value alone is difficult for layout engineer to act on for any layout fix. When these checks fail, the resistance is reported for the failing source/sink pair, but a single resistance value does not guide how to fix it. A physical layer change will need to occur to fix it, but that single value provides no guidance on where to look and what to do, and that is especially problematic on complex paths that can span dozens of physical layers. Ultimately this can lead to design delays and even failing silicon.

IC Validator PERC

IC Validator™ PERC is part of the more prominent IC Validator physical verification solution. IC Validator provides industry-leading solutions for DRC, LVS, FILL, pattern matching, and many other applications.

IC Validator PERC leverages StarRC™ for R-extraction and Python for a rich programming environment, and together those are the technology backbone for the flow. That flow can then be used for netlist checks, netlist driving layout DRC checks, P2P, and current density.

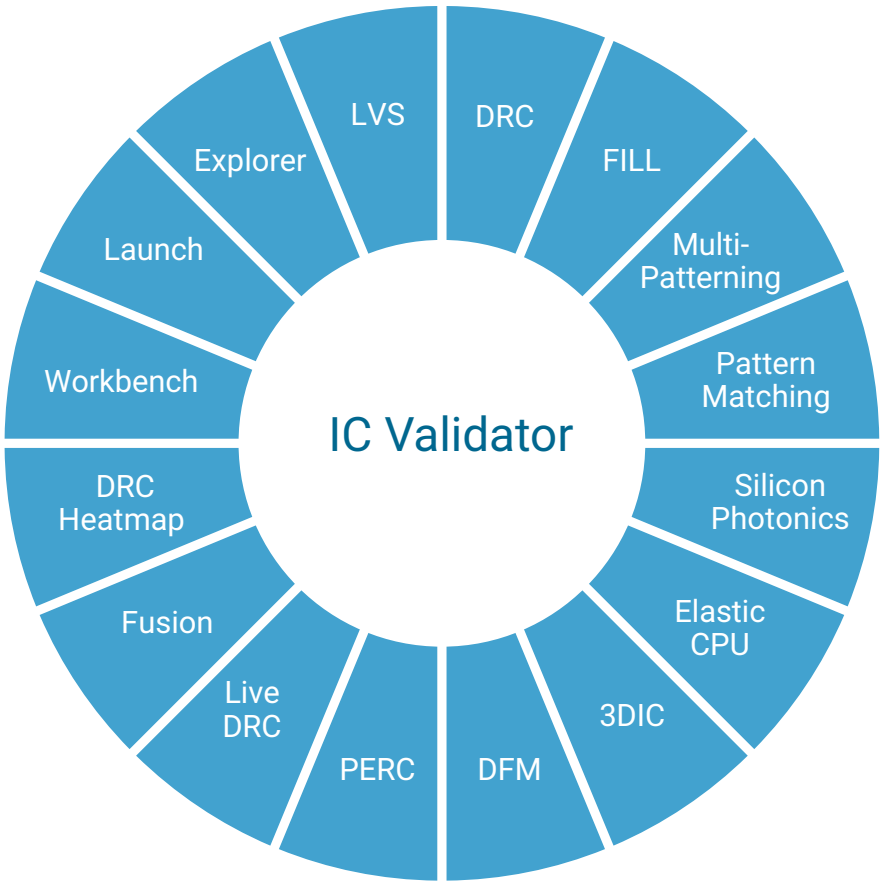

Figure 1: IC Validator Physical Verification Solution

IC Validator PERC is qualified for significant foundry ESD/LUP checking of P2P resistance measurement, even at the full-chip level. IC Validator PERC P2P flow employs StarRC for R extraction, which is the industry gold standard. To provide better P2P resistance analysis for the layout engineer to act when there is a P2P resistance violation, IC Validator PERC offers a distinctive feature to analyze P2P resistance result contribution by layer. This feature enables beneficial information for the user to decide which interconnect layers are high contributors to be the candidates for layout fix.

Enabling IC Validator PERC Collecting Database for P2P Resistance Contribution by Layer

To use this debug capability, R reduction will need to be turned off in the P2P resistance flow. The reason is that reduction greatly simplifies the R network, and information about the actual fractured layout polygons is lost. This control is in the StarRC tech file, and the IC Validator PERC flow has a mechanism to define rules to PERC that then get passed into StarRC. The “readme” for your foundry runset for P2P resistance would provide the information needed to do this.

Performance Impact of Producing Data for P2P Resistance Contribution by Layer

If the user is only running PERC P2P on IO nets and other non-P/G nets, then enabling P2P resistance contribution by layer will have minimal impact on performance. However, if the user is running PERC P2P, including P/G nets, then the user should expect a performance impact, depending on the size of the design. This performance impact is insignificant if the design is small (chip size is less than a few mm^2). If the chip size is larger than 10 mm^2, the performance cost will be more significant due to StarRC not reducing the R network of the P/G nets. The chip size estimation for performance cost is a rough guide to keep in mind and not a hard rule.

Using IC Validator VUE to Access P2P Resistance Contribution by Layer in Conjunction with Layout Highlighting

The user can launch IC Validator PERC job as usual. Upon the successful completion of IC Validator PERC P2P job, the user will be able to analyze P2P resistance contribution by layer in IC Validator VUE together with a layout viewer supported by IC Validator VUE. In the below section, the debug process in conjunction with P2P resistance contribution by layer is described. The user starts a layout viewer such as IC Validator WorkBench, Virtuoso, or Custom Compiler™. With the layout database open, the user invokes IC Validator VUE and loads topcell.vue file. Select "PERC Errors" tab to point to IC Validator PERC P2P run results; the violation P2P paths associated with each check name are listed on the Violation Browser page (on the left panel of VUE main window). Select one of the paths, and more details are shown as Violation Details/Description (on the right panel of VUE main window). Select the top line for each path in the Violation Details panel, right-click to drop-down list of can-do function, select (left click) on "PERC Path Heatmap," and then a "Highlight Path" dialog window pops out. In the top portion of "Highlight Path" dialog window, there are list of symbols. Select the rightmost symbol (looks like a table), the P2P resistance contribution by layer table named "Contribution to Path Resistance" is shown. Each of these steps in the VUE debug procedures to access P2P resistance contribution by layer is displayed in figure 2.

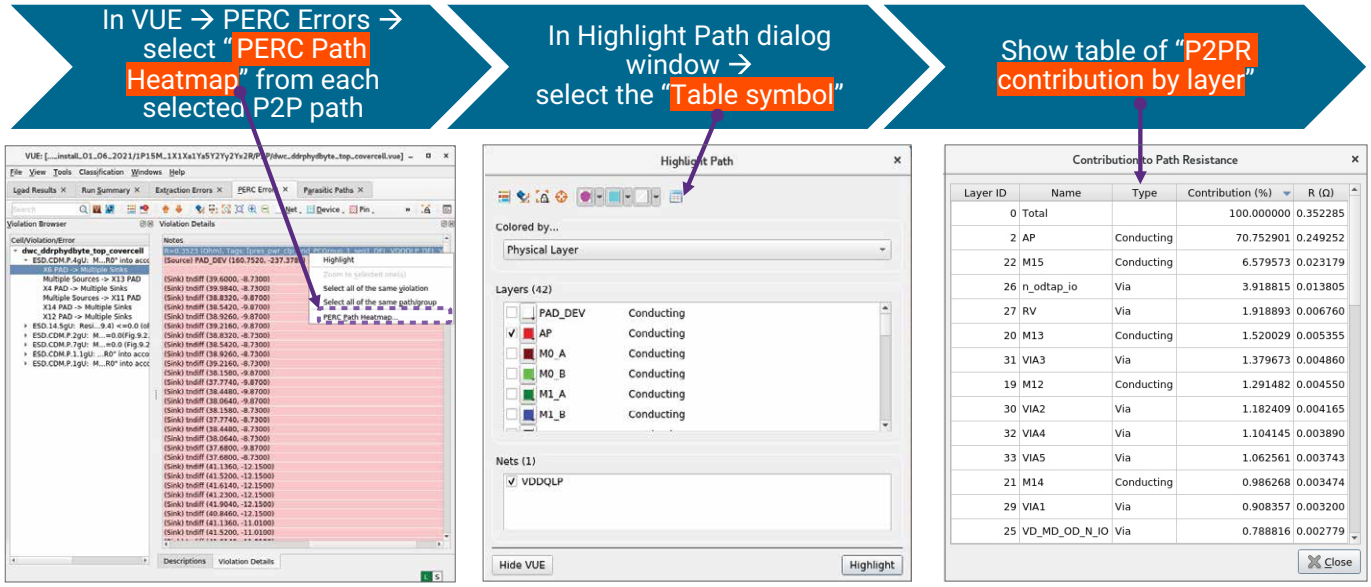

Figure 2: A flow chart describes accessing P2P resistance contribution by layer in VUE.

The P2P resistance contribution by layer data (named as Contribution to Path Resistance table) provides how the lumped total resistance of the selected P2P path is summed up from various layers. Since each layer has its sheet resistance, layout polygons alone can't tell the user what to do. The top contributors of resistance combined with layer polygon highlight capability in the "Highlight Path" dialog window give the layout engineer a much better idea of what to do for a layout fix. Figure 3 shows one P2P path measured from ESD diodes one physical power Pad of a power net.

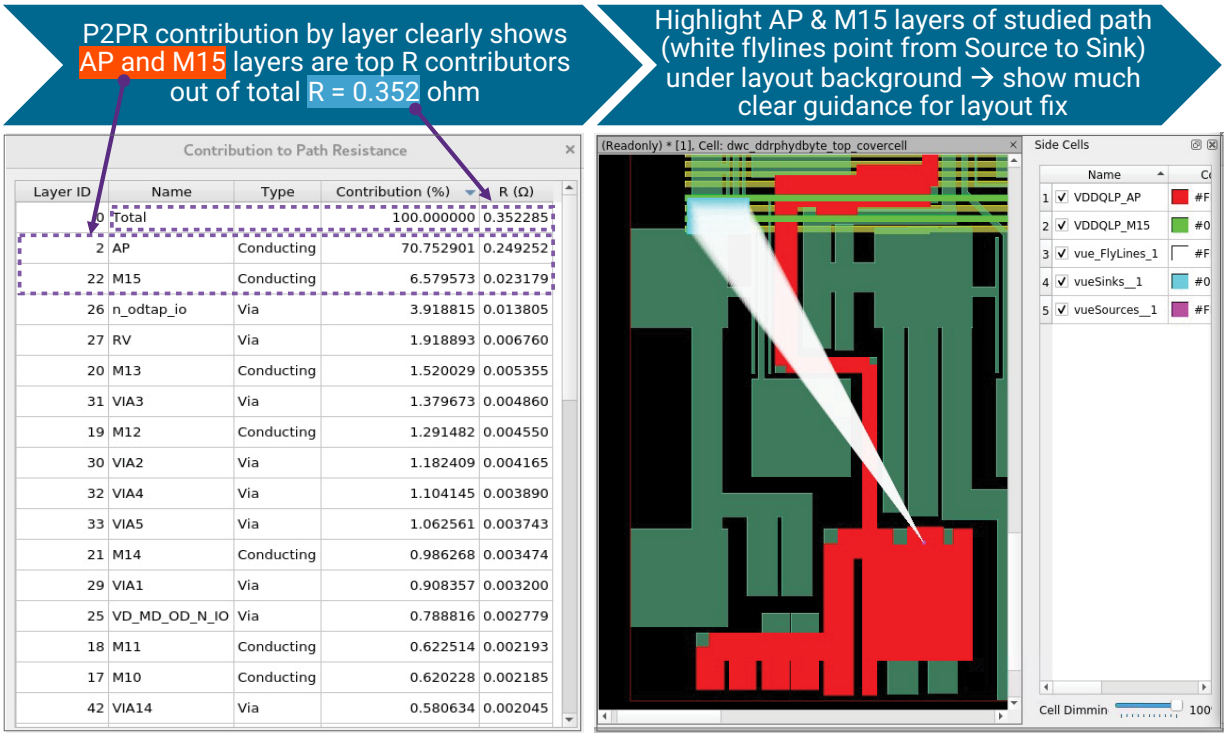

Figure 3: Pictures show how P2P resistance contribution by layer table provides valuable information for a user to focus debug and layout fix priority

Interpreting Contribution by Layer Results to Fix Design Issues

Fixing P2P resistance issues in a design can be a complex problem. Proper fixing depends most heavily on the designer's knowledge of their design and what changes they can make to resolve it. Additional information like a contribution by layer is intended to help understand the results more effectively so that the designer can apply their design knowledge with more confidence and greater speed. So, for example, knowing that the top thick metal represents 70% of the P2P resistance contribution does show what to change with that metal routing. But it does indicate quickly to a design whether the results are as expected or whether something unusual has occurred. And it gives confidence for the designer to make changes to the top think metal knowing that there will not be unintended consequences for that changes.

Summary

Point-to-point resistance checking is an essential component of robust ESD design verification. However, debugging the reported errors can be a real challenge and frustration to ESD engineers. IC Validator PERC provides the "contribution by layer" feature in its P2P Heatmap interface to IC Validator VUE, which offers tremendous insight into fixing these critical design errors. This saves time in the design cycle and gives higher confidence going into silicon ESD testing.

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